(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 073 123 A2

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
31.01.2001 Bulletin 2001/05

(51) Int Cl.[7]: **H01L 29/06**, H01L 29/78

(21) Application number: **00306444.1**

(22) Date of filing: **28.07.2000**

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: **29.07.1999 JP 21531899**

(71) Applicant: **KABUSHIKI KAISHA TOSHIBA**
Kawasaki-shi, Kanagawa-ken (JP)

(72) Inventor: **Yasuhara, Norio,**
c/o Intellectual Property Div.
Minato-ku, Tokyo 105-8001 (JP)

(74) Representative: **Granleese, Rhian Jane**
Marks & Clerk,
57-60 Lincoln's Inn Fields
London WC2A 3LS (GB)

(54) High withstand voltage semiconductor device

(57) A plurality of trenches (12) are formed in a drift region between a p-type body region (2) and an-type buffer region (4) A silicon oxide film (13) is formed on the side and bottom of each of the trenches (12), and an SIPOS film (14) is buried into each of the trenches. The trenches (12) are formed by RIE, and the SIPOS film (14) is deposited by LPCVD and an undesired portion can be removed by dry etching such as RIE. The SIPOS film (14) is connected to a source electrode (7) at the source end of each trench (12), and it is connected to a drain electrode (8) directly or through a resistor at the drain end thereof. When a high voltage is applied, a depletion layer expands in the n-type drift region (6) from an interface between the n-type drift region (6) and the trench (12) on each side of the n-type drift region (6), therefore, the impurity concentration of the n-type drift region (6) can be heightened without lowering the high breakdown voltage, and the resistance of the drift region can be decreased.

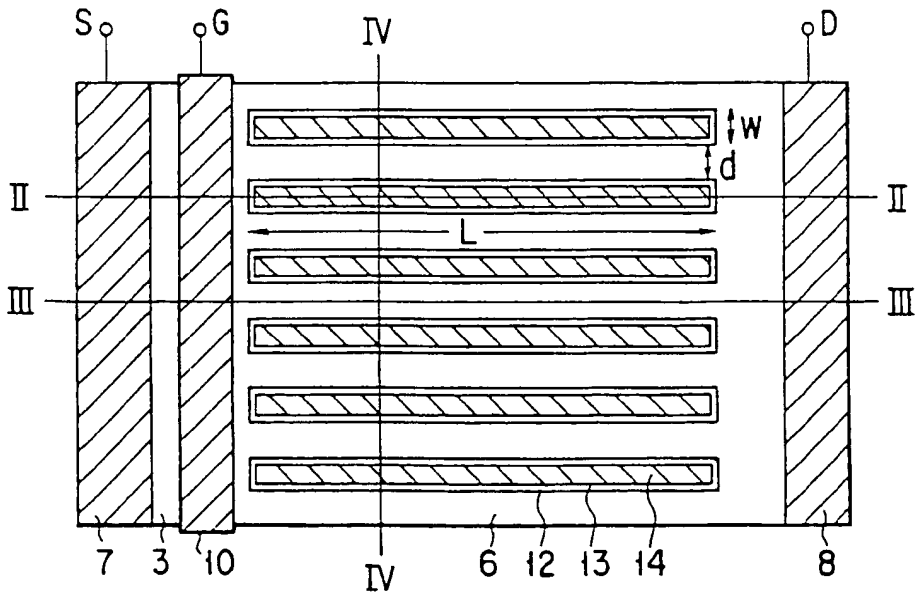


FIG. 1

EP 1 073 123 A2

Description

[0001] The present invention relates to a high breakdown voltage semiconductor device and, more specifically, to a technique of reducing the resistance of a drift region of a high breakdown voltage MOSFET.

[0002] A high breakdown voltage semiconductor device, such as a high breakdown voltage MOSFET and IGBT, has a drift region whose impurity concentration is relatively low in order to obtain a high breakdown voltage. If a high voltage is applied to the element in an off state, the drift region is depleted and the element withstands the high voltage. Since the drift region is low in impurity concentration, it increases in resistance and has a large share of on-resistance of the element. As the breakdown voltage heightens, the drift region increases in resistance; accordingly, the on-resistance of the element increases.

[0003] A high breakdown voltage MOSFET, which has the structure as shown in FIG. 20 to decrease the resistance of a drift region, is proposed in T. Fujihira, "Theory of Semiconductor Superjunction Devices," Jpn. J. Appl. Phys., Vol. 36 (1997), pp 6254-6262. In this MOSFET, a drift region 43 is formed between a p-type body region 41 and an n^+-type drain region 42 in order to obtain a high breakdown voltage. The drift region 42 is constituted of p-type layers 44 and n-type layers 45 which are arranged alternately at small pitches in the channel width direction. If a high voltage is applied between the source and drain so as to make the drain positive, a depletion layer expands not only from both a pn junction between the p-type body region 41 and n-type layers 45 and a pn junction between a p-type layer 46 and the n-type layers 45, but also from a pn junction between the p-type layers 44 and n-type layers 45. For this reason, even though the impurity concentration of the n-type layers 45 is set higher than that of the drift region of a normal high breakdown voltage MOSFET, the n-type layers 45 can be depleted and the breakdown voltage can be maintained. With the structure of the MOSFET shown in FIG. 20, therefore, the resistance of the drift region can be lowered by increasing the impurity concentration of the n-type layers 45.

[0004] However, in order to achieve the above advantage, the impurity concentration of the n-type layers 45 has to be at least two times as high as that of the normal high breakdown voltage MOSFET, provided that the P- and n-type layers 44 and 45 have the same width a. In order to prevent the breakdown voltage from lowering in this state, the width a need to be reduced and the depth b of the layers 44 and 45 need to be increased to some extent. For example, the depth b should be 2 μm at the minimum when the width a is 1 μm. To reduce the on-resistance to half by the same breakdown voltage as that of the normal MOSFET, the depth b should be about 4 μm at the minimum when the width a is 1 μm. Such a structure is difficult to achieve by the current manufacturing technique and, if it is done, its manufacture process will be complicated and increased in cost.

[0005] As described above, there is a problem in which the conventional superjunction elements are difficult to manufacture in actuality.

[0006] The present invention has been developed in consideration of the above situation and its object is to provide a high breakdown voltage semiconductor device which is easy to manufacture and low in on-resistance.

[0007] According to a first aspect of the present invention, there is provided a high breakdown voltage semiconductor device formed on a high resistance semiconductor layer, comprising a plurality of trenches formed like a stripe in a drift region in substantially parallel with a current flowing direction, an insulation film formed on a side and a bottom of each of the trenches, and a high resistance film buried into each of the trenches with the insulation film interposed therebetween, wherein the high resistance film is connected to one of source and gate electrodes directly or through a resistor near a source-end portion of each of the trenches, and the high resistance film is connected to a drain electrode directly or through a resistor near a drain-end portion of each of the trenches.

[0008] In the high breakdown voltage semiconductor device according to the first aspect of the present invention, the high resistance film may be formed on one of a semi-insulating polycrystalline silicon and polysilicon.

[0009] According to a second aspect of the present invention, there is provided a high breakdown voltage semiconductor device formed on a high resistance semiconductor layer of a first conductivity type, comprising a drift region of a second conductivity type selectively formed on a surface of the high resistance semiconductor layer, a plurality of trenches formed like a stripe in the drift region in substantially parallel with a current flowing direction, an insulation film formed on a side and a bottom of each of the trenches, and a high resistance film buried into each of the trenches with the insulation film interposed therebetween, wherein the high resistance film is connected to one of source and gate electrodes directly or through a resistor near a source-end portion of each of the trenches, and the high resistance film is connected to a drain electrode directly or through a resistor near a drain-end portion thereof.

[0010] In the high breakdown voltage semiconductor device according to the second aspect of the present invention, the high resistance film may be formed on one of a semi-insulating polycrystalline silicon and polysilicon.

[0011] According to a third aspect of the present invention, there is provided a high breakdown voltage semiconductor device including a first high breakdown voltage MOSFET, a second high breakdown voltage MOSFET, a resistor, comprising a plurality of trenches formed like a stripe in a drift region of the first high breakdown voltage MOSFET, in substantially parallel with a current flowing direction, an insulation film formed on a

side and a bottom of each of the trenches, and a high resistance film buried into each of the trenches with the insulation film interposed therebetween, wherein the first high breakdown voltage MOSFET and the second high breakdown voltage MOSFET have a common source electrode and a common gate electrode, and one end of the high resistance film is connected to the common gate electrode, while another end thereof is connected to a drain electrode of the second high breakdown voltage MOSFET and one end of the resistor.

[0012] In the high breakdown voltage semiconductor device according to the third aspect of the present invention, the high resistance film may be formed on one of a semi-insulating polycrystalline silicon and polysilicon.

[0013] In the high breakdown voltage semiconductor device according to the third aspect of the present invention, the first high breakdown voltage MOSFET and the second high breakdown voltage MOSFET may be formed in a common semiconductor layer. The high resistance film may be formed on one of a semi-insulating polycrystalline silicon and polysilicon.

[0014] According to a fourth aspect of the present invention, there is provided a high breakdown voltage semiconductor device formed on a high resistance semiconductor layer, comprising, a plurality of trenches formed like a stripe in a drift region in substantially parallel with a current flowing direction, an insulation film formed on a side of each of the trenches, and a high resistance film buried into each of the trenches, wherein the high resistance film is connected to one of source and gate electrodes directly or through a resistor near a source-end portion of each of the trenches, and the high resistance film is connected to a drain region near a drain-end portion of each of the trenches.

[0015] In the high breakdown voltage semiconductor device according to the fourth aspect of the present invention, the high resistance film may be formed on one of a semi-insulating polycrystalline silicon and polysilicon.

[0016] In the high breakdown voltage semiconductor device according to the present invention, a drift region is divided into a plurality of long regions each interposed between a plurality of trenches, and a depletion layer expands in a drift region from an interface between the drift region and each of the trenches when a reversed bias is applied. Thus, the impurity concentration of the drift region can be normally heightened to cause a high breakdown voltage. Consequently, the on-resistance can be lowered by increasing the impurity concentration of the drift region.

[0017] This summary of the invention does not necessarily describe all necessary features so that the invention may also be a sub-combination of these described features.

[0018] The invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

FIG. 1 is a plan view showing a high breakdown voltage MOSFET according to a first embodiment of the present invention;

FIG. 2 is a cross-sectional view taken along line II-II of FIG. 1;

FIG. 3 is a cross-sectional view taken along line III-III of FIG. 1;

FIG. 4 is a cross-sectional view taken along line IV-IV of FIG. 1;

FIG. 5 is a cross-sectional view showing a high breakdown voltage MOSFET according to a second embodiment of the present invention;

FIG. 6 is a cross-sectional view partly showing a high breakdown voltage MOSFET according to the second embodiment of the present invention;

FIG. 7 is a cross-sectional view showing a high breakdown voltage MOSFET according to a third embodiment of the present invention;

FIG. 8 is a plan view showing a high breakdown voltage MOSFET according to a fourth embodiment of the present invention;

FIG. 9 is a plan view showing a high breakdown voltage MOSFET according to a fifth embodiment of the present invention;

FIG. 10 is a cross-sectional view taken along line X-X of FIG. 9;

FIG. 11 is a cross-sectional view taken along line XI-XI of FIG. 9;

FIG. 12 is a cross-sectional view taken along line XII-XII of FIG. 9;

FIG. 13 is a cross-sectional view taken along line XIII-XIII of FIG. 9;

FIG. 14 is an illustration of a high breakdown voltage semiconductor device according to a sixth embodiment of the present invention;

FIG. 15 is a plan view of the high breakdown voltage semiconductor device according to the sixth embodiment of the present invention;

FIG. 16 is a plan view showing a high breakdown voltage MOSFET according to a seventh embodiment of the present invention;

FIG. 17 is a cross-sectional view taken along line XVII-XVII of FIG. 16;

FIG. 18 is a cross-sectional view taken along line XVIII-XVIII of FIG. 16;

FIG. 19 is a cross-sectional view showing a high breakdown voltage MOSFET according to an eighth embodiment of the present invention; and

FIG. 20 is a cross-sectional view of a prior art superjunction high breakdown voltage MOSFET.

[0019] Embodiments of the present invention will now be described with reference to the accompanying drawings.

[0020] FIGS. 1 to 4 show the main part of a lateral n-channel high breakdown voltage MOSFET according to a first embodiment of the present invention. FIG. 1 is a plan view thereof, and FIGS. 2 to 4 are cross-sectional

views taken along lines II-II, III-III and IV-IV of FIG. 1, respectively. Please note that FIG. 1 does not show an insulation film 11 in order to present the layout of electrodes on an active layer.

[0021] A p-type body region 2 is formed selectively on the surface of a high-resistance p^--type layer 1 made of monocrystalline silicon, and an n^+-type source region 3 having a high impurity concentration is formed in the surface area of the body region 2. An n-type buffer region 4 is formed on the surface of the layer 1 at a given distance from the region 2, and an n^+-type drain region 5 having a high impurity concentration is formed in the surface area of the buffer region 4. An n-type drift region 6 is formed between the p-type body region 2 and n-type buffer region 4 in order to obtain a high breakdown voltage. The dose of impurities of the n-type drift region 6 is 2×10^{12} cm^{-2} to 2×10^{13} cm^{-2}. The impurity concentration of the n-type buffer region 4 is higher than that of the n-type drift region 6, and the region 4 is provided for the purpose of relieving the concentration of electric fields and decreasing the resistance but not necessarily required. A source electrode 7 is formed on the p-type body region 2 so as to be connected with both the body region 2 and source region 3, and a drain electrode 8 is formed on the n^+-type drain region 5. A gate electrode 10 is provided on the surface of the p-type body region 2 between the regions 3 and 6, with a gate oxide film 9 interposed therebetween. The surface of the resultant structure is protected by the insulation film 11 such as a silicon oxide film

[0022] A plurality of trenches 12 are formed in the drift region 6 between the regions 2 and 4. A silicon oxide film 13 having a thickness of 5 to 100 nm is formed on the sides and bottom of each of the trenches 12, and a semi-insulating polycrystalline silicon (SIPOS) film 14 having a high resistance is buried therein. The trenches 12 are formed by RIE (Reactive Ion Etching), the SIPOS film 14 is deposited by LPCVD, and an undesired portion is removed by dry etching such as RIE and CDE (Chemical Dry Etching). The trenches 12 each have a width w of 0.3 μm to 1 μm, and the distance d between adjacent trenches is 0.5 μm to 5 μm. The length L of each trench is equal to that of the drift region 6 and set in accordance with the breakdown voltage of the device. If the breakdown voltage is 500 V, the length L is about 50 μm. The depth of the trenches 12 is substantially equal to that of the drift region 6. As diagrammatically shown in FIG. 2, the SIPOS film 14 is connected to the source electrode 7 at the source-side ends of the trenches 12 and it is connected to the drain electrode 8 at the drain-side ends thereof. The SIPOS film 14 can be connected to the gate electrode 10 at the source-ends. The resistance of the film 14 can be adjusted by the concentration of oxygen contained therein and the dimensions of the trenches 12. The most of the drift region 6 is divided into a plurality of long portions by the trenches 12. The section of FIG. 3, which shows not the trenches 12 but the portion obtained by dividing the drift region 6, corresponds to that of a normal high-breakdown voltage MOSFET having no trenches. If, in the normal high-breakdown voltage MOSFET, a high voltage is applied in the OFF state, a depletion layer expands in an n-type drift region and a p^--type layer to relieve the concentration of electric fields and thus to obtain a high breakdown voltage.

[0023] In the above high breakdown voltage MOSFET of the first embodiment, if a voltage is applied between the drain and source so as to set the drain at a high potential, the potentials corresponding to the voltage are distributed in the SIPOS film 14 in each of the trenches 12. In that part of the n-type drift region 6 which is interposed between two adjacent trenches 12, a depletion layer expands not only from a pn junction between the part and the p^--type layer 1 or p-type body region 2, but also from an interface between the part and each of the trenches 12. The n-type drift region 12 is depleted more easily than in the structure with no trenches. Even though the impurity concentration of the n-type drift region 6 is set higher than the optimum value in the device having no trenches, the drift region 6 will be depleted. Thus, the impurity concentration of the drift region 6 can be increased without lowering the breakdown voltage. Consequently, the resistance of the drift region can be decreased, as can be the on-resistance of the high breakdown voltage MOSFET. If the width w of each trench 12 is 1 μm, the distance d between adjacent trenches is 1 μm, and the depth thereof is about 4 μm, the impurity concentration of the n-type drift region 6 can be about four times as high as that in the device with no trenches, and the resistance of the drift region can be reduced to half. Similarly, the resistance of the drift region can be reduced to half even if the width w and distance d are each 0.5 μm and the depth is about 1 μm. The trenches 12 having such dimensions can be formed by conventional lithography or RIE. If the width w and distance d are further decreased and the depth of the trenches are further increased, the dose of impurities of the n-type drift region 6 can be increased more than 2×10^{13} cm^{-2}. It is advisable that the thickness of the silicon oxide film 13 be about one sixth of the distance d between the trenches 12.

[0024] In the first embodiment, the SIPOS film 14 is buried into each of the trenches 12; however, it can be replaced with polysilicon whose impurity concentration is low.

[0025] A high breakdown voltage MOSFET according to a second embodiment of the present invention is illustrated in FIG. 5 corresponding to FIG. 2 showing that of the first embodiment. In the second embodiment, a resistor 15 is inserted between the drain-side end of the SIPOS film 14 and the drain electrode 8. In order to make the impurity concentration of the n-type drift region 6 as high as possible, the values of the resistor 15 can be adjusted to control the distribution of potentials caused on the SIPOS film 14. Similarly, a resistor can be inserted between the source-side end of the SIPOS film 14 and the source electrode 7 (or gate electrode

10), though not shown.

[0026] The high breakdown voltage MOSFET of the second embodiment can actually be constituted as illustrated in FIG. 6. FIG. 6 is a cross-sectional view of the structure of the periphery of the drain. The drain-side end of the SIPOS film 14 is extended and connected to the drain electrode 8 directly. That portion of the SIPOS film 14 which extends from the drain electrode 8 to the trenches 12 (i.e., the extended portion of the film 14) serves as the resistor 15.

[0027] FIG. 7 is a plan view showing the major part of a high breakdown voltage MOSFET according to a third embodiment of the present invention. The sections taken along lines II-II, III-III, IV-IV in FIG. 7 correspond to those of FIGS. 2, 3 and 4, respectively. In the third embodiment, the trenches 12 are decreased in width on the drain side. If the n-type drift region 6 is thickened on the drain side, the breakdown voltage can be higher than that of the first embodiment. The same breakdown voltage increases the total amount of impurity of the n-type drift region 6 and lowers the on-resistance further.

[0028] FIG. 8 is a plan view showing the major part of a high breakdown voltage MOSFET according to a fourth embodiment of the present invention. The sections taken along lines II-II, III-III, IV-IV in FIG. 8 correspond to those of FIGS. 2, 3 and 4, respectively. In the fourth embodiment, the trenches 12 are decreased in width gradually from the source toward the drain. As in the third embodiment, the breakdown voltage can be higher than that of the first embodiment. The same breakdown voltage increases the total amount of impurity of the n-type drift region 6 and lowers the on-resistance further.

[0029] FIGS. 9 to 13 illustrate the major part of a high breakdown voltage MOSFET according to a fifth embodiment of the present invention. FIG. 9 is a plan view thereof, and FIGS. 10 to 13 are cross-sectional views taken along lines X-X, XI-XI, XII-XII and XIII-XIII of FIG. 9, respectively. In the fifth embodiment, a second n-type drift region 16 is provided in the drift region 6 near the drain. The dose of the second drift region 16 is substantially the same as that of the drift region 6, and the depth thereof is equal to or greater than that of the drift region 6. As in the third and fourth embodiments, the breakdown voltage can be made higher than that in the first embodiment by diffusing more impurities into the drain side of the n-type drift region than the source side thereof. The same breakdown voltage increases the total amount of impurity of the n-type drift region and lowers the on-resistance further.

[0030] FIGS. 14 and 15 are illustrations of a high breakdown voltage semiconductor device according to a sixth embodiment of the present invention. The device of the sixth embodiment includes the same high-breakdown voltage MOSFET T1 as that of the first embodiment, a second high-breakdown voltage MOSFET T2, and a resistor R1. However, the SIPOS film 14 and drain electrode 8 are not directly connected to each other. FIG. 14 shows that a load is connected to these constituting elements. The MOSFET T1 is illustrated by the sectional view corresponding to FIG. 2 of the first embodiment. FIG. 15 shows one example of the plane structure for accomplishing the structure shown in FIG. 14, and not any loads.

[0031] As in the first embodiment, a plurality of trenches 12 are formed in the drift region of the first high-breakdown voltage MOSFET T1 serving as the main element. The SIPOS film 14 is buried into each of the trenches 12, and one of the film 14 is connected to the gate electrode 10 of the MOSFET T1, while the other end thereof is connected to the drain electrode 17 of the second high-breakdown voltage MOSFET T2 and one end of the resistor R1. The sources of the first and second MOSFETs T1 and T2 are connected to each other, as are the gates thereof. The first and second MOSFETs T1 and T2 are designed so as to have substantially the same breakdown voltage. However, the second MOSFET T2 may have a high on-resistance. The other end of the resistor R1 is connected to a high-voltage DC power supply Vdd. A load is connected between the drain electrode 8 of the MOSFET T1 and the DC power supply Vdd.

[0032] Assuming that the operation voltage Vg of the gate is 5 V and the DC power supply voltage Vdd is 200 V, the first MOSFET T1 usually necessitates a breakdown voltage of about 400 V and the drift region requires a length of about 40 μm. If the resistance of the resistor R1 is r1, the resistance of parallel connection of all the SIPOS films 14 is r2, and the on-resistance of the second MOSFET T2 is r3, r1:r2:r3 is, for example, 39:3900:1. It is desirable that the absolute value of these resistances be larger.

[0033] When the gate is turned on by applying a 5V-voltage thereto, the drain voltage $\underline{v}$ of the MOSFET T2 is set to 5V and so is the potential of all the SIPOS films 14, since the ratio of r1 to r3 is 39:1 (=(Vdd-Vg):Vg). Thus, electrons are induced on the sides of the trenches 12 to form a storage layer and decrease the drift resistance further, with the result that the on-resistance of the entire MOSFET T1 is lowered. The ratio of r1 to r3 need not be 39:1 strictly and if it is not too small, the same advantage can be obtained. If the ratio of r1 to r3 is set larger than that of (Vdd-Vg) to Vg, the advantage of causing the storage form to be formed becomes greater. However, the drain voltage $\underline{v}$ has to be used within such a range that it exceeds a voltage of the trenches 12 or a voltage corresponding to the gate breakdown voltage.

[0034] When the gate is turned off, the same condition is obtained as in the second embodiment and the potentials are distributed on the SIPOS film in accordance with the ratio of r1 to r2. The potential at the drain-side end of the SIPOS film 14 is close to that of the drain, and the potential at the gate-side end thereof is equal to that of the gate. A potential gradient occurs on the entire SIPOS film 14 such that the potential increases gradually from the gate toward the drain. As compared

with a device having no trenches, not only the breakdown voltage of the MOSFET T1 can be maintained, but also it can be increased further. Like in the first embodiment, a depletion layer expands from the interface between the n-type drift region 6, which is interposed between adjacent two trenches 12, and each side of the trench 12, so that the impurity concentration of the drift region 6 can be increased.

[0035] Consequently, according to the sixth embodiment, the resistance of the drift region can be lowered by the two advantages: the impurity concentration of the drift region 6 can be set high, and electrons are induced on the sides of the trench 12 to cause a storage layer.

[0036] In the sixth embodiment, the high breakdown voltage MOSFET of the third to fifth embodiments can be used for the MOSFET T1.

[0037] FIGS. 16 to 18 show the major part of a high breakdown voltage MOSFET according to a seventh embodiment of the present invention. FIG. 16 is a plan view thereof, and FIGS. 17 and 18 are cross-sectional views taken along lines XVII-XVII and XVIII-XVIII of FIG. 16, respectively. In the seventh embodiment, the device of the first embodiment is modified and formed on an SOI substrate. A buried oxide film 19 is formed on a silicon substrate 18, and a high-resistance n^--type layer 20 is formed thereon. The same high breakdown voltage MOSFET as that of the first embodiment is formed on the SOI substrate. As in the first embodiment, the impurity concentration of the n-type drift region 6 can be heightened without lowering the breakdown voltage; therefore, the drift region can be decreased in resistance. The n^--type layer 20 can be replaced with a high-resistance p-type layer.

[0038] FIG. 19 is a cross-sectional view showing the major part of a vertical high-breakdown voltage MOSFET to which the present invention is applied as an eighth embodiment. An n-type drift layer 21 is formed in a monocrystalline silicon active layer, and a p-type body region 22 is formed selectively in the surface region of the drift layer 21. A high impurity concentration n^+-type source region 23 is formed on the surface region of the region 22. A high impurity concentration n^+-type drain region 24 is formed on the opposite surface of the drift layer 21. A source electrode 25 is formed on the p-type body region 22 so as to connect with both the regions 22 and 23, and a drain electrode 26 is formed in the n^+-type drain region 24. A gate electrode 28 is provided on the surface of the p-type body region 22, which is interposed between the n^+-type source region 23 and n-type drift layer 21, with a gate oxide film 27 therebetween.

[0039] A plurality of trenches 29 are formed in the n-type drift layer 21 to such a depth as to reach the n^+-type drain region 24. A silicon oxide film 30 having a thickness of about 5 nm to 100 nm is formed on the side wall of each of the trenches 29, and a high-resistance SIPOS film 31 is buried therein. The trenches 29 need not necessarily reach the n^+-type drain region. The SIPOS film 31 is connected to the n^+-type drain region 24 at the bottom and connected to the source electrode 25 on the top. In the eighth embodiment, too, a depletion layer expands from the interface between the n-type drift layer 21 and each of the trenches 29 in the drift layer 21 when a high voltage is applied, so that the impurity concentration of the drift layer 21 can be increased without lowering the breakdown voltage, thus decreasing the resistance of the drift layer.

[0040] An example where the present invention is applied to an n-channel high breakdown voltage MOSFET, has been described. It is needless to say that the present invention can be applied to a p-channel high breakdown voltage MOSFET. It can also be applied to another high breakdown voltage semiconductor device such as IGBT. The device can be constituted to have a trench gate like that shown in FIG. 20.

[0041] As a film to be buried in the trenches, a low impurity concentration polysilicon film can be used in place of the SIPOS film, as can be another high-resistance film.

[0042] According to the high breakdown voltage semiconductor device described above, the impurity concentration of the drift region can be heightened and the on-resistance can be lowered by decreasing the drift resistance.

Claims

1. A high breakdown voltage semiconductor device formed on a high resistance semiconductor layer, characterized by comprising:

   a plurality of trenches (12) formed like a stripe in a drift region (6) in substantially parallel with a current flowing direction;
   an insulation film (13) formed on a side and a bottom of each of the trenches; and
   a high resistance film (14) buried into each of the trenches with the insulation film interposed therebetween,

   wherein the high resistance film (14) is connected to one of source and gate electrodes (7, 10) directly or through a resistor near a source-end portion of each of the trenches (12), and the high resistance film (14) is connected to a drain electrode (8) directly or through a resistor near a drain-end portion of each of the trenches (12).

2. A high breakdown voltage semiconductor device formed on a high resistance semiconductor layer of a first conductivity type, characterized by comprising:

   a drift region (6) of a second conductivity type selectively formed on a surface of the high resistance semiconductor layer;

a plurality of trenches (12) formed like a stripe in the drift region in substantially parallel with a current flowing direction;
an insulation film (13) formed on a side and a bottom of each of the trenches; and
a high resistance film (14) buried into each of the trenches with the insulation film interposed therebetween,

wherein the high resistance film (14) is connected to one of source and gate electrodes (7, 10) directly or through a resistor near a source-end portion of each of the trenches (12), and the high resistance film (14) is connected to a drain electrode (8) directly or through a resistor near a drain-end portion thereof.

3. A high breakdown voltage semiconductor device including a first high breakdown voltage MOSFET (T1), a second high breakdown voltage MOSFET (T2), a resistor (R1), characterized by comprising:

a plurality of trenches (12) formed like a stripe in a drift region (6) of the first high breakdown voltage MOSFET, in substantially parallel with a current flowing direction;
an insulation film (13) formed on a side and a bottom of each of the trenches; and
a high resistance film (14) buried into each of the trenches with the insulation film interposed therebetween,

wherein the first high breakdown voltage MOSFET (T1) and the second high breakdown voltage MOSFET (T2) have a common source electrode (7) and a common gate electrode (10), and one end of the high resistance film (14) is connected to the common gate electrode (10), while another end thereof is connected to a drain electrode of the second high breakdown voltage MOSFET and one end of the resistor (R1).

4. The high breakdown voltage semiconductor device according to claim 3, the first high breakdown voltage MOSFET (T1) and the second high breakdown voltage MOSFET (T2) are formed in a common semiconductor layer.

5. A high breakdown voltage semiconductor device formed on a high resistance semiconductor layer, characterized by comprising:

a plurality of trenches (12) formed like a stripe in a drift region (6) in substantially parallel with a current flowing direction;
an insulation film (13) formed on a side of each of the trenches; and
a high resistance film (14) buried into each of the trenches,

wherein the high resistance film (14) is connected to one of source and gate electrodes (7, 10) directly or through a resistor near a source-end portion of each of the trenches (12), and the high resistance film (14) is connected to a drain region (8) near a drain-end portion of each of the trenches (12).

6. The high breakdown voltage semiconductor device according to claim 1, characterized in that the high resistance film (14) is formed on one of a semi-insulating polycrystalline silicon and polysilicon.

7. The high breakdown voltage semiconductor device according to claim 2, characterized in that the high resistance film (14) is formed on one of a semi-insulating polycrystalline silicon and polysilicon.

8. The high breakdown voltage semiconductor device according to claim 3, characterized in that the high resistance film (14) is formed on one of a semi-insulating polycrystalline silicon and polysilicon.

9. The high breakdown voltage semiconductor device according to claim 4, characterized in that the high resistance film (14) is formed on one of a semi-insulating polycrystalline silicon and polysilicon.

10. The high breakdown voltage semiconductor device according to claim 5, characterized in that the high resistance film (14) is formed on one of a semi-insulating polycrystalline silicon and polysilicon.

FIG. 1

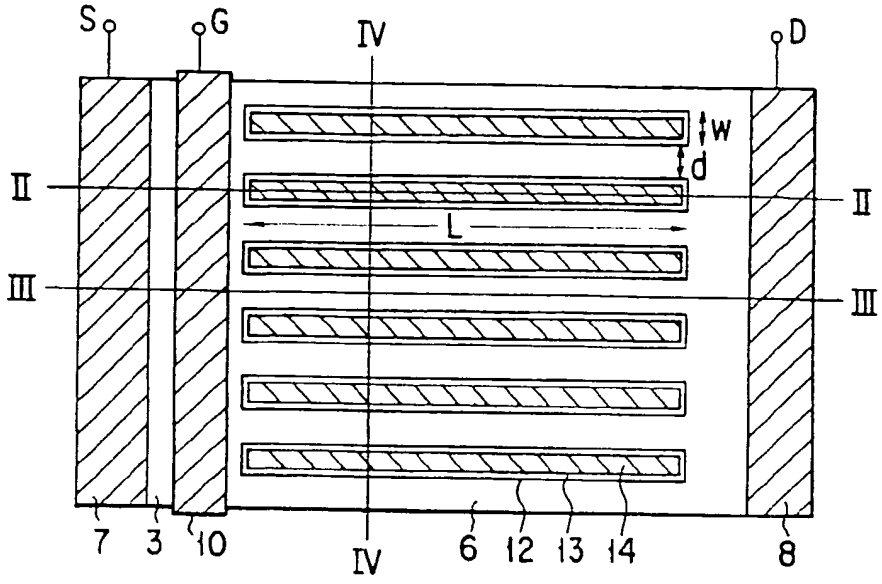


FIG. 2

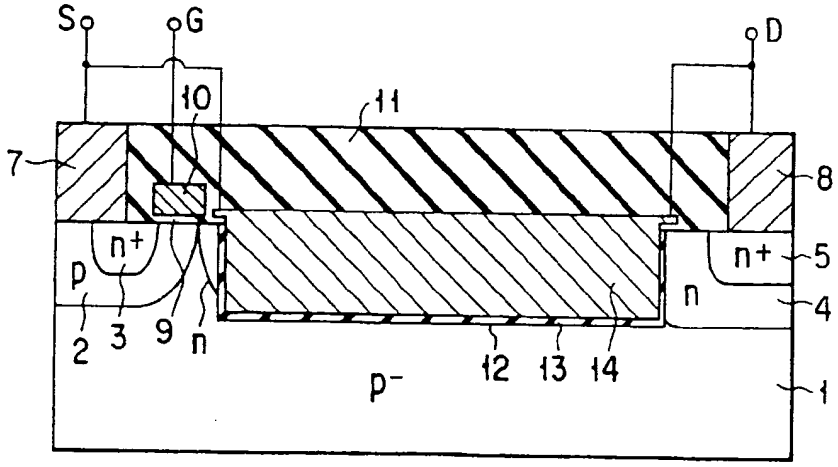
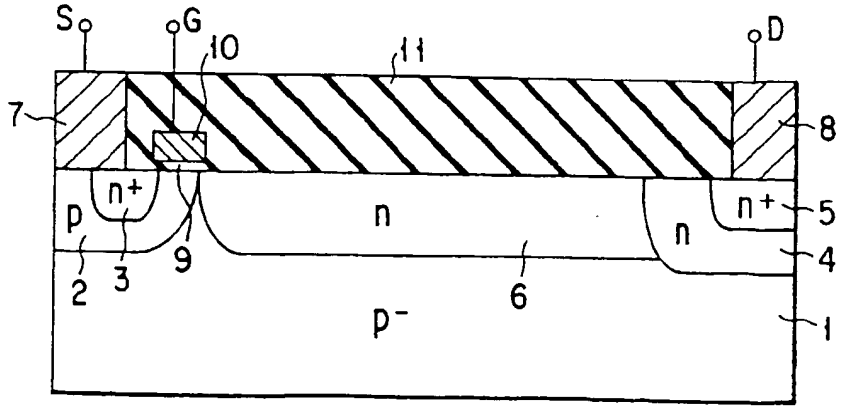


FIG. 3



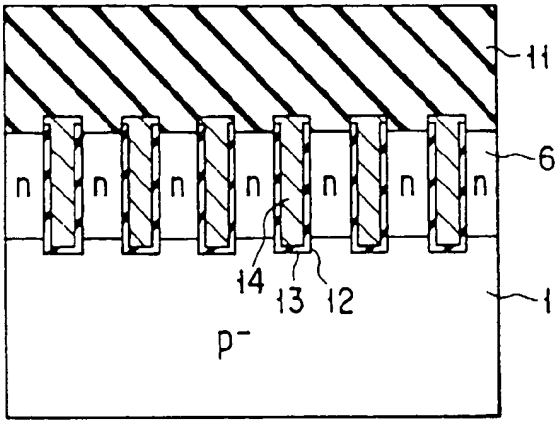


FIG. 4

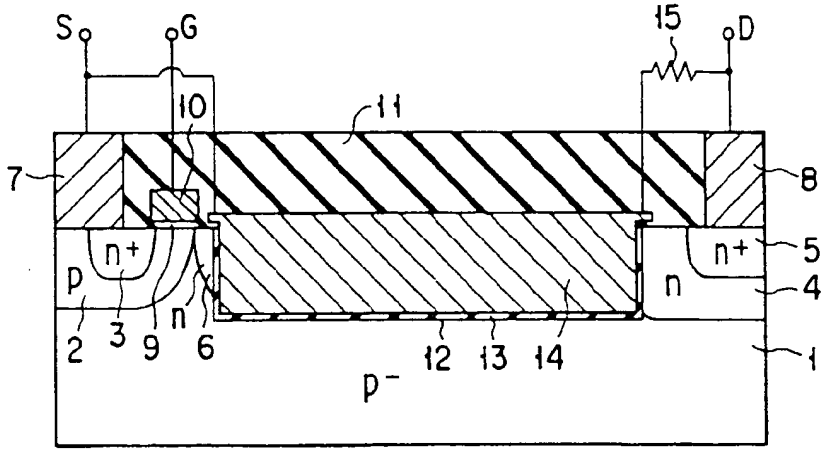


FIG. 5

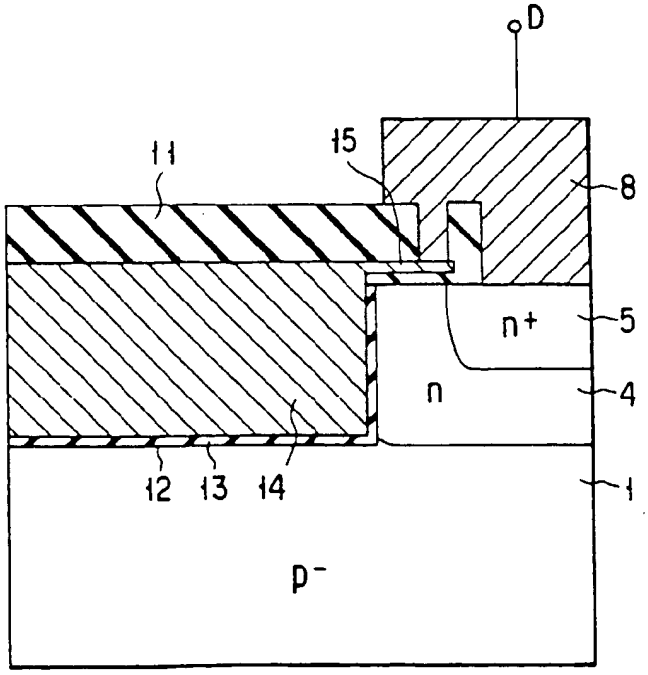


FIG. 6

FIG. 7

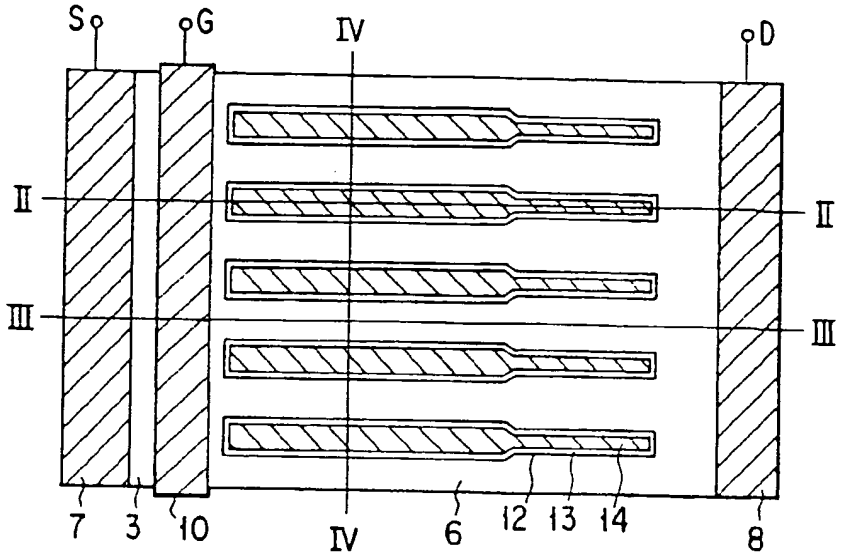


FIG. 8

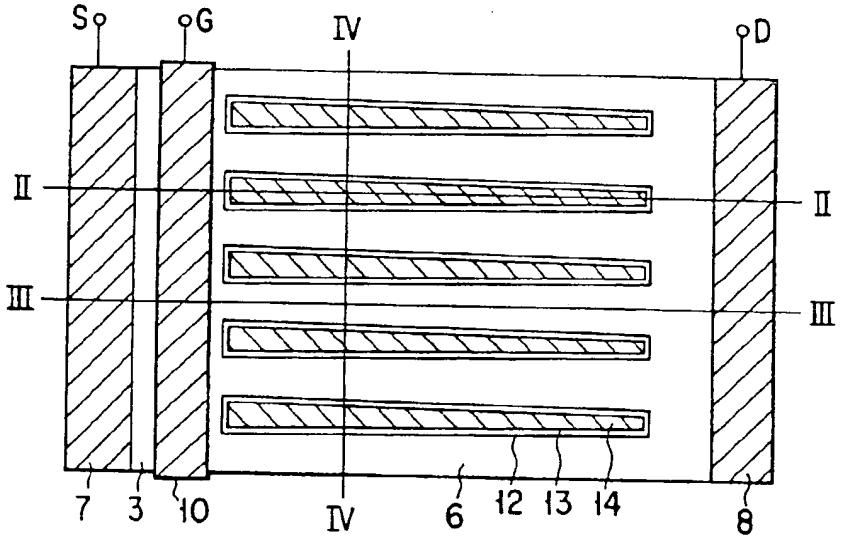
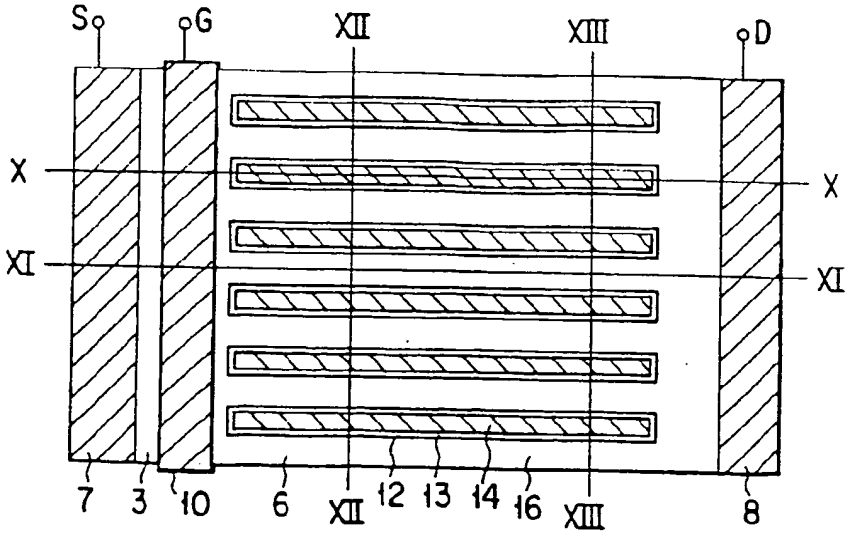


FIG. 9



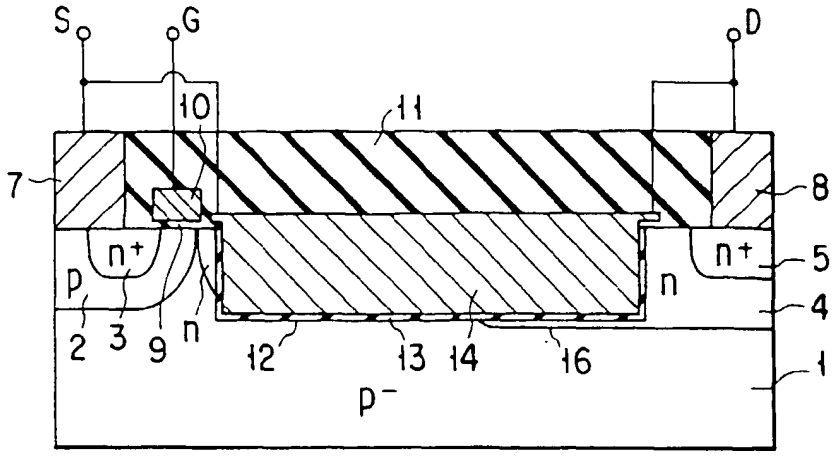


FIG. 10

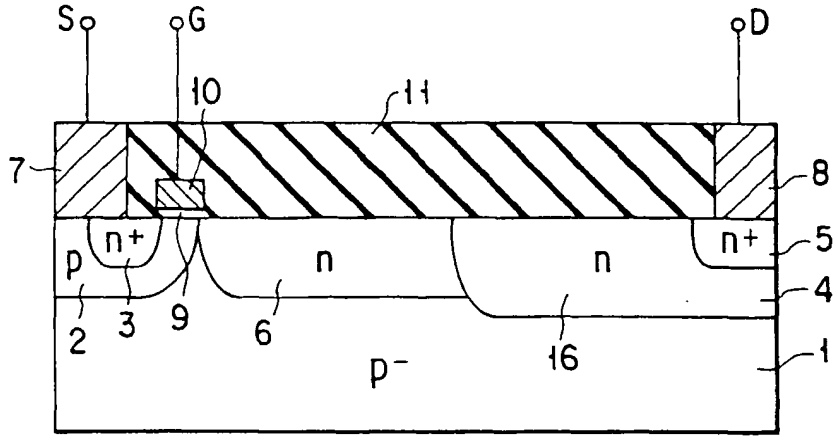


FIG. 11

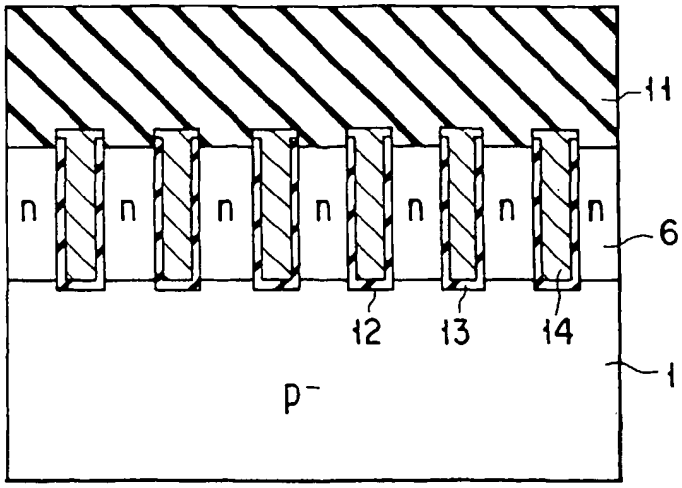


FIG. 12

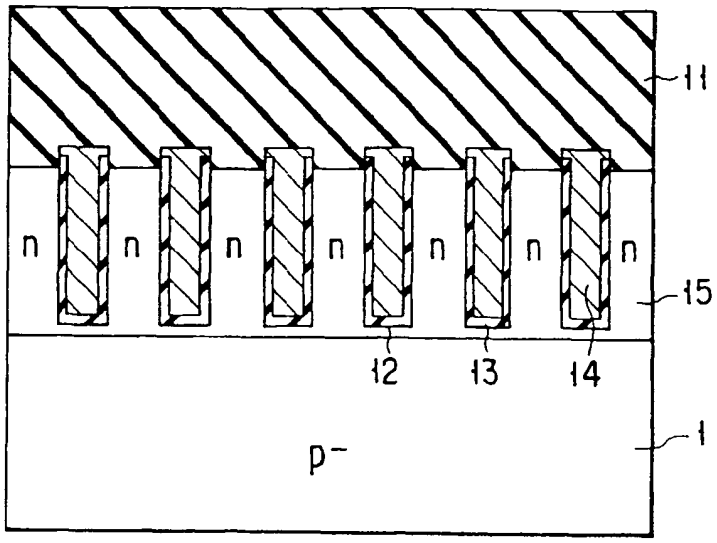

11
n
n
n
n
n
n
n
15
12
13
14
p-
1

FIG. 13

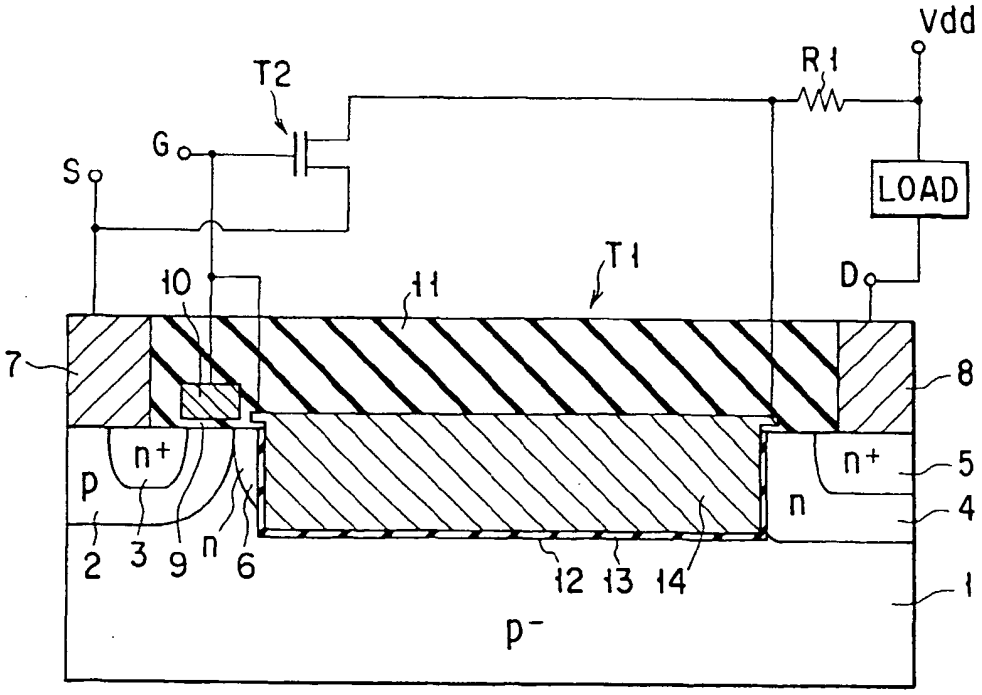

Vdd
R1
T2
G
S
LOAD
T1
D
10
11
7
8
n+
p
n+
5
n
4
2
3
9
n
6
12
13
14
1
p-

FIG. 14

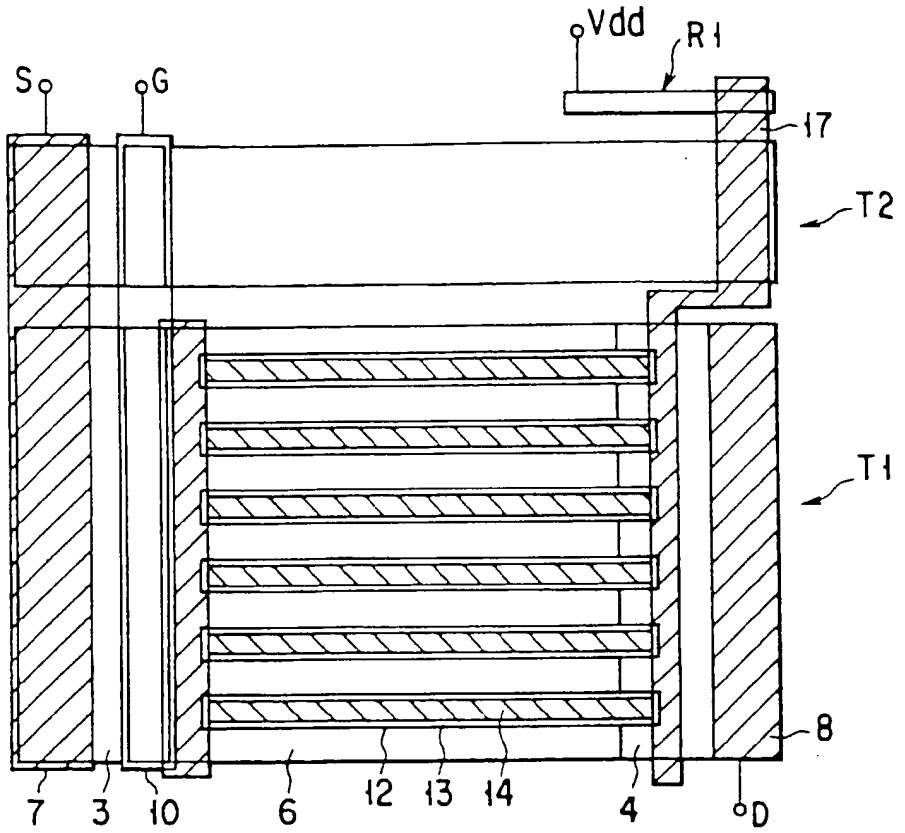

Vdd
R1
S
G
17
T2
T1
8
7
3
10
6
12
13
14
4
D

FIG. 15

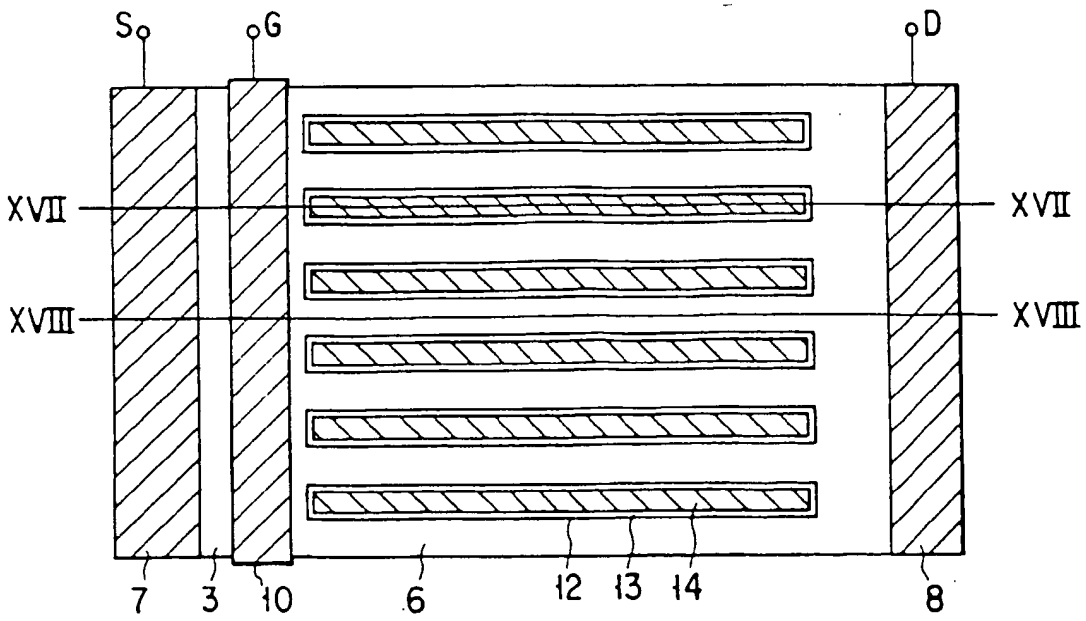

S
G
D
XVII
XVII
XVIII
XVIII
7
3
10
6
12
13
14
8

FIG. 16

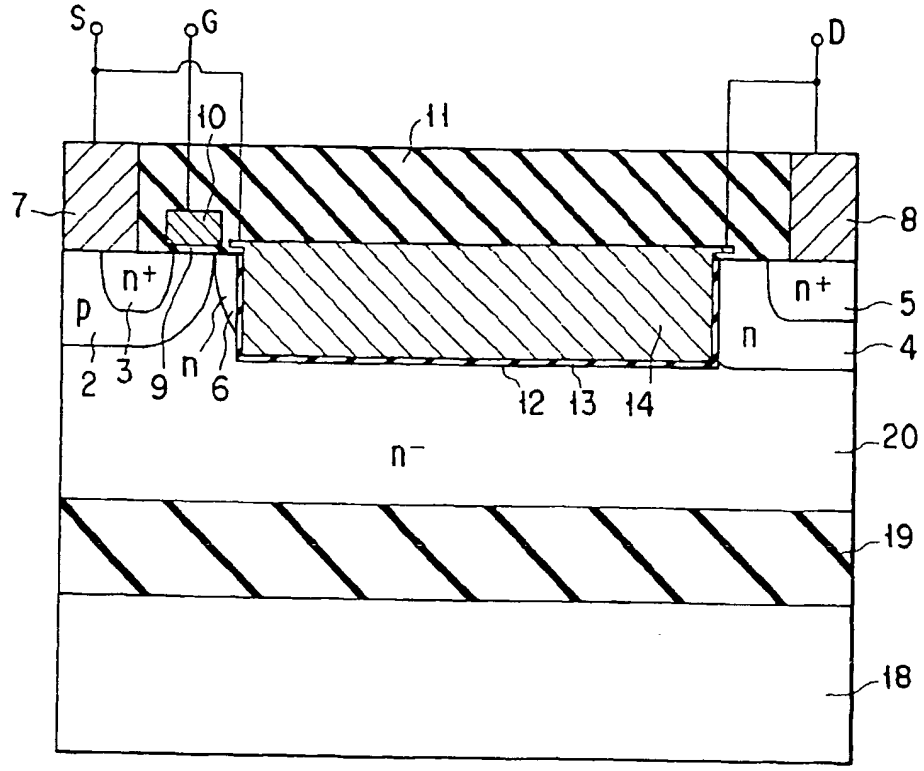

S
G
D
10
11
7
8
n+
p
n+
5
n
4
2
3
9
n
6
12
13
14
n−
20
19
18

FIG. 17

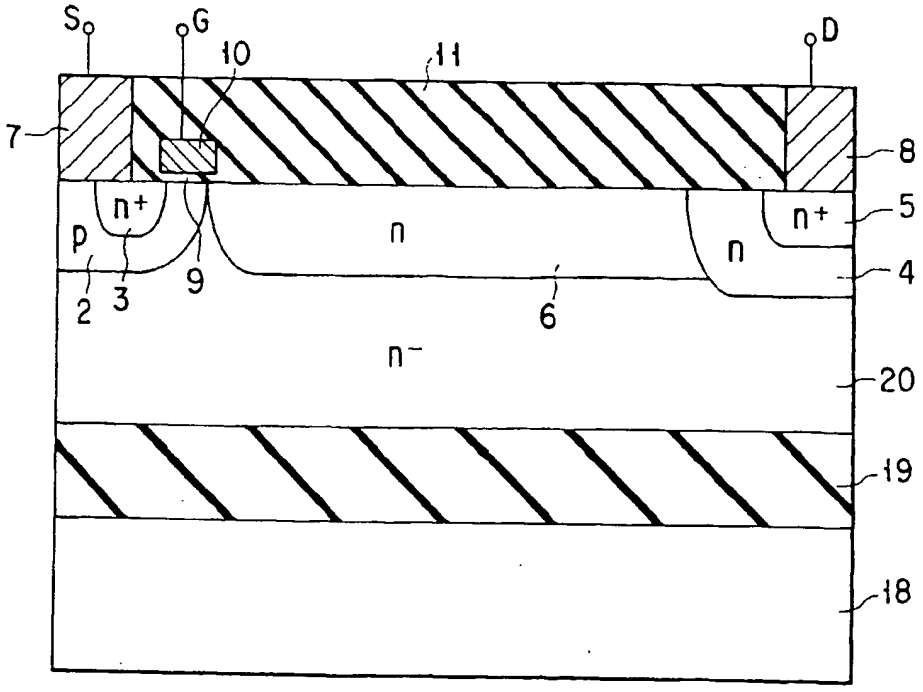

S
G
D
10
11
7
8
n+
p
n
n+
5
n
4
2
3
9
6
n−
20
19
18

FIG. 18

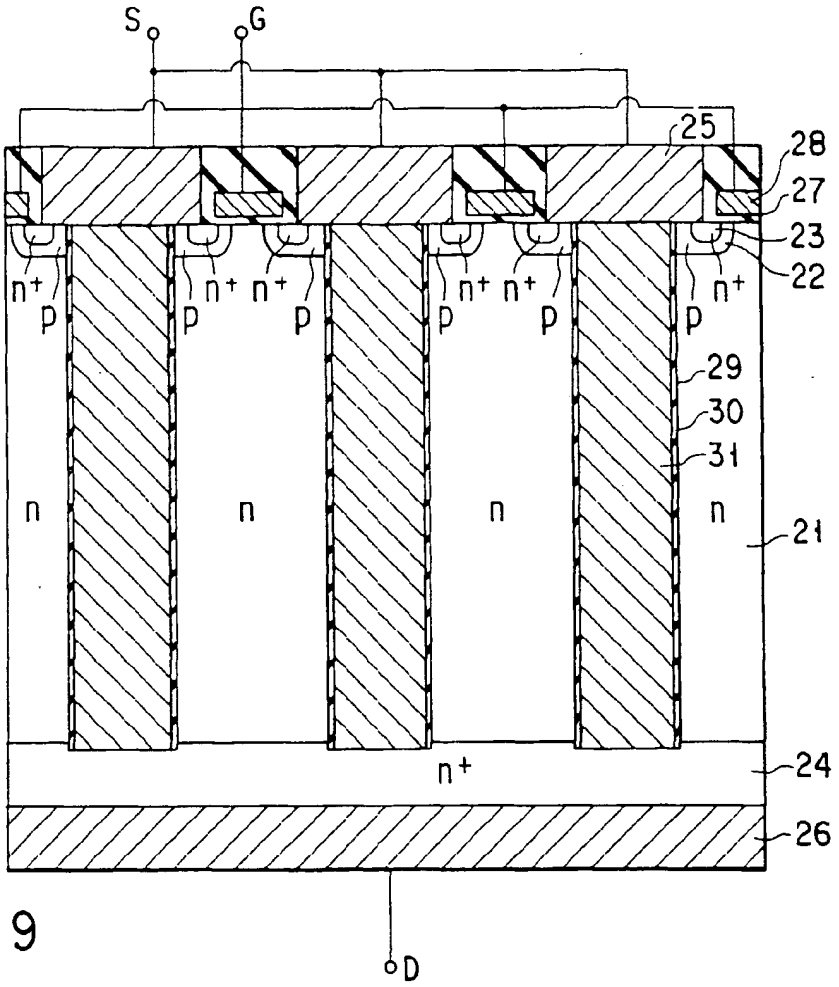

S
G
25
28
27
23
22
n+
p
n
29
30
31
21
24
26
D

FIG. 19

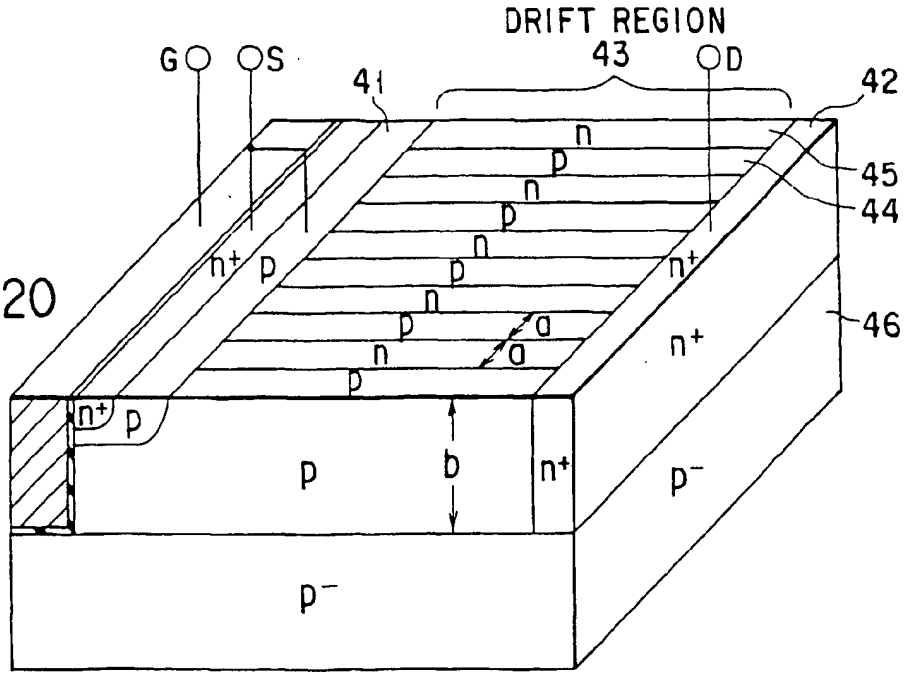

DRIFT REGION
G
S
41
43
D
42
45
44
46
n
p
n+
a
b
p−

FIG. 20

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 073 123 A3

(12) EUROPEAN PATENT APPLICATION

(88) Date of publication A3:
23.05.2001 Bulletin 2001/21

(43) Date of publication A2:
31.01.2001 Bulletin 2001/05

(21) Application number: **00306444.1**

(22) Date of filing: **28.07.2000**

(51) Int Cl.[7]: **H01L 29/78**, H01L 29/41, H01L 29/49, H01L 27/06

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: **29.07.1999 JP 21531899**

(71) Applicant: **KABUSHIKI KAISHA TOSHIBA**
Kawasaki-shi, Kanagawa-ken (JP)

(72) Inventor: **Yasuhara, Norio,**
c/o Intellectual Property Div.
Minato-ku, Tokyo 105-8001 (JP)

(74) Representative: **Granleese, Rhian Jane**
Marks & Clerk,
57-60 Lincoln's Inn Fields
London WC2A 3LS (GB)

(54) High withstand voltage semiconductor device

(57) A plurality of trenches (12) are formed in a drift region between a p-type body region (2) and an-type buffer region (4). A silicon oxide film (13) is formed on the side and bottom of each of the trenches (12), and an SIPOS film (14) is buried into each of the trenches. The trenches (12) are formed by RIE, and the SIPOS film (14) is deposited by LPCVD and an undesired portion can be removed by dry etching such as RIE. The SIPOS film (14) is connected to a source electrode (7) at the source end of each trench (12), and it is connected to a drain electrode (8) directly or through a resistor at the drain end thereof. When a high voltage is applied, a depletion layer expands in the n-type drift region (6) from an interface between the n-type drift region (6) and the trench (12) on each side of the n-type drift region (6), therefore, the impurity concentration of the n-type drift region (6) can be heightened without lowering the high breakdown voltage, and the resistance of the drift region can be decreased.

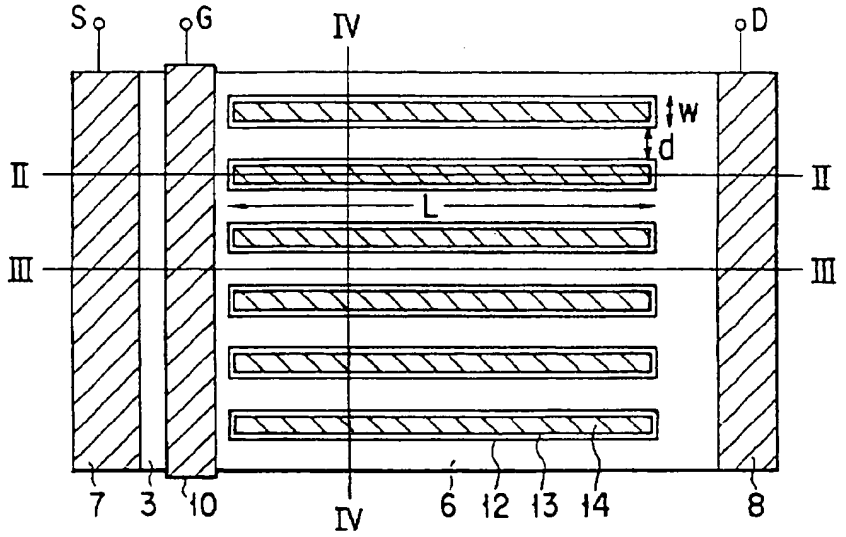


FIG. 1

EP 1 073 123 A3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 00 30 6444

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	GB 2 089 118 A (PHILIPS ELECTRONIC AND ASSOCIATED INDUSTRIES LTD) 16 June 1982 (1982-06-16)	5,10	H01L29/78 H01L29/41 H01L29/49
A	* page 2, line 15 - page 3, line 32; figure 1 * * page 3, line 100 - page 4, line 14; figure 4 *	1-3,6-9	H01L27/06
A	US 4 947 232 A (ASHIDA T ET AL) 7 August 1990 (1990-08-07) * column 2, line 46 - column 3, line 29; figure 1 *	1-3,5-10	
A	US 4 796 070 A (BLACK R D) 3 January 1989 (1989-01-03) * column 6, line 15 - column 9, line 15; figures 1-7 *	1-3,5-10	
P,X	DE 198 48 828 A (SIEMENS AG) 4 May 2000 (2000-05-04)	5,10	
P,A	* column 5, line 18 - line 32; figure 4 * * column 4, line 20 - line 21 *	1-3,6-9	TECHNICAL FIELDS SEARCHED (Int.Cl.7)
D,A	FUJIHIRA T: "THEORY OF SEMICONDUCTOR SUPERJUNCTION DEVICES" JAPANESE JOURNAL OF APPLIED PHYSICS, PART 1, vol. 36, no. 10, October 1997 (1997-10), pages 6254-6262, XP000918328 TOKYO, JP ISSN: 0021-4922		H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
MUNICH	28 March 2001	Morvan, D

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 00 30 6444

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

28-03-2001

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
GB 2089118 A	16-06-1982	NONE	
US 4947232 A	07-08-1990	JP 1396916 C	24-08-1987
		JP 56133870 A	20-10-1981
		JP 62002705 B	21-01-1987
		JP 1396917 C	24-08-1987
		JP 56133871 A	20-10-1981
		JP 62002706 B	21-01-1987
US 4796070 A	03-01-1989	NONE	
DE 19848828 A	04-05-2000	NONE	